Aaron Dingler
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I. **EDUCATION**

2013 – PhD in Computer Science and Engineering, University of Notre Dame, Notre Dame, IN
2012 – MS in Computer Science and Engineering, University of Notre Dame, Notre Dame, IN
2007 – BS in Computer Engineering, University of Notre Dame, Notre Dame, IN

II. **ACADEMIC APPOINTMENTS**

08/13- **SEATTLE PACIFIC UNIVERSITY**   **Seattle, WA**
Present

   a. Teaching Responsibilities
   I am responsible for teaching a broad range of courses in the CSC and CPE
   curriculum. This includes the following recurring courses:
   CSC 1010 – Fall 2013, Fall 2014, Fall 2015
   CSC 1230 – Fall 2013, Spring 2014, Fall 2014, Fall 2015, Winter 2016
   CSC 2430 – Winter 2015, Spring 2015
   CSC/CPE/EE 3760 – Winter 2014, Winter 2015, Winter 2016
   CSC/CPE 4760 – Spring 2014
   CSC/CPE 4750 – Spring 2015
   CSC 3011/3899 – Fall 2014, Winter 2016

   And the following independent study, directed research and special topics offerings:
   CSC 2951 – Fall 2015
   CSC 3930 – Fall 2015
   CSC 3940 – Fall 2015
   CSC 4800 – Spring 2014
   CSC 4970 – Winter 2015, Spring 2015, Fall 2015

   b. Administrative Responsibilities
   Computer Engineering Coordinator, 2014-present
   Advisor, SPU IEEE club, 2015-present
   Advisor, SPU Computer Science Club (SPU Developers), 2015-present

   c. University Governances or other committees
   Admission, Advising, and Retention Committee, 2014-2017

III.   PEER REVIEWED PUBLICATIONS

[1] R. Perricone, Y. Liu, **A. Dingler**, X. S. Hu and M. Niemier, "Design of Stochastic Computing Circuits Using Nanomagnetic Logic," in *IEEE Transactions on Nanotechnology*, vol. 15, no. 2, pp. 179-187, March 2016.

[2] M. Niemier, G. Csaba, **A. Dingler**, X.S. Hu, W. Porod, X. Ju, M. Becherer, D. Schmitt-Landsiedel, and P. Lugli. Boolean and non-boolean nearest neighbor architectures for out-of-plane nanomagnet logic. In Cellular Nanoscale Networks and Their Applications (CNNA), 2012 13th International Workshop on, pages 1–6, August 2012.

[3] **A. Dingler**, S. Kurtz, M. Niemier, X. S. Hu, G. Csaba, J. Nahas, W. Porod, G. Bernstein, P. Li, and V. K. Sankar. Making Non-Volatile Nanomagnet Logic Non-Volatile. In Proceedings of the 49th Annual Design Automation Conference, DAC '12, pages 476–485, June 2012.

[4] M.T. Niemier, E. Varga, G. H. Bernstein, W. Porod, M.T. Alam, **A. Dingler**, A. Orlov, and X.S. Hu. Shape Engineering for Controlled Switching With Nanomagnet Logic. IEEE Transactions on Nanotechnology, 11(2):220 –230, March 2012.

[5] **A. Dingler**, M. T. Niemier, X. S. Hu, and E. Lent. Performance and Energy Impact of Locally Controlled NML Circuits. Journal of Emerging Technologies in Computing Systems, 7(1):1–24, 2011.

[6] **A. Dingler**, M. Niemier, X. S. Hu, M. Garrison, and M. T. Alam. System-Level Energy and Performance Projections for Nanomagnet-based Logic. In NANOARCH '09: Proceedings of the 2009 IEEE/ACM International Symposium on Nanoscale Architectures, pages 21–26, 2009.

[7] **A. Dingler**, M. J. Siddiq, M. Niemier, X. S. Hu, M. T. Alam, G. Bernstein, and W. Porod. Controlling Magnetic Circuits: How Clock Structure Implementation will Impact Logical Correctness and Power. In DFT '09: Proceedings of the 2009 24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, pages 94–102, 2009.

[8] M. Niemier, X.S. Hu, **A. Dingler**, M.T. Alam, G. Bernstein, and W. Porod. Bridging the Gap between Nanomagnetic Devices and Circuits. In ICCD '08: Proceedings of the 2008 IEEE International Conference on Computer Design, 2008, pages 506–513, Oct. 2008.

[9] M. Niemier, **A. Dingler**, and X. S. Hu. Design Tradeoffs for Improved Performance in MQCA-Based Systems. In NDCS '08: Proceedings of the 2008 IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems, pages 35–38, 2008

IV.   ACADEMIC PEER-REVIEWED PRESENTATIONS
- Making Non-volatile Nanomagnet Logic Non-volatile. Talk and Poster, Device Automation Conference (DAC). June 6, 2012.
- Nanomagnet Logic: From Devices to Architectures. Poster, SIGDA Ph.D. Forum (Co-located with DAC). June 5, 2012.
- How Clock Structure Implementation Impacts Logical Correctness and Power

Consumption in Nanomagnetic Logic. Talk, Defect and Fault Tolerance in VLSI Systems (DFT '09). October 7, 2009.
- How Design Parameters Can Affect Performance in MQCA-Based Systems. Talk, International Workshop on Design and Test of Nano Devices, Circuits and Systems (NDCS). September 29, 2008.

V. OTHER: INVITED PRESENTATIONS, PANELS AND PROFESSIONAL WORKSHOPS
- Panelist at TEALs event at Microsoft's Redmond campus spring 2014, spring 2015.

VI. PEER REVIEW EXPERIENCE*
- ACM Journal of Emerging Technologies in Computing (JETC)
- Consortium for Computing Sciences in Colleges Northwestern Regional Conference (CCSC-NW)
- IEEE Transactions on Computers (TC)
- IEEE International Conference on Nanotechnology (NANO)
- IEEE Transactions on Nanotechnology (TNANO)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- Journal of Computational Electronics

*listed alphabetically

VII. AWARDS AND GRANTS
- SPU Faculty Research Grant, Summer 2015.
- Best Paper, NANOARCH 2009 [6].
- Outstanding Graduate Student Teacher Award for Excellence in Teaching, Fall 2009.

VIII. RELATED WORK EXPERIENCE
- Computer science camp instructor for middle school students at Eastside Catholic School, Summer 2014, 2015.

IX. PROFESSIONAL ASSOCIATIONS
- Member, Institute for Electrical and Electronics Engineers.
- Member, Association for Computing Machinery.